



PATENT

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AFIN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Serial No.: 10/615,042)
)
Filed: July 8, 2003)
)
Art Unit: 2815)
)
Examiner: Jesse A. Fenty)
)
For: COPPER-LOW-K DUAL)
DAMASCENE)
INTERCONNECT WITH)
IMPROVED RELIABILITY)
)
Inventors: Valeriy Sukharev et al.)
)
Attorney Ref: 03-0509)

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450, on May 10, 2005.


James R. Foley

TRANSMITTAL OF APPEAL BRIEF

Mail Stop: Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Appellant submits herewith in triplicate the Appeal Brief in the above-captioned application with respect to the Notice of Appeal filed on May 3, 2005.

This Appeal Brief is on behalf of other than a small entity. As such, pursuant to 37 CFR 1.17(f), the fee for filing the Appeal Brief is for other than a small entity in the amount of \$500.00.

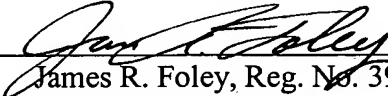
The total fee due for the filing of this Appeal Brief is \$500.00. Please charge Deposit Account No. 12-2252 in the amount of \$500.00 in payment of the fee for filing this Appeal Brief. A duplicate copy of this Transmittal is attached.

Even though Appellant believes that no extension of time is required, Conditional

Petition is made to provide for the possibility that Appellant inadvertently overlooked a need for a petition and fee for extension of time. If any other fee is required, Appellant authorizes the Commissioner to charge such fee to their deposit account number 12-2252.

Respectfully submitted,

Date: May 10, 2005

By: 
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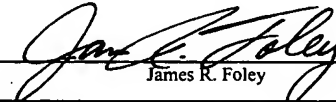


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James R. Foley

APPEAL BRIEF

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The above-captioned patent application is respectfully submitted to the Honorable Board of Patent Appeals and Interferences after final rejection by Examiner Jesse A. Fenty, Group Art Unit 2815, refusing allowance of the claims as presented and amended in the above-captioned patent application. A copy of the claims in issue is included herewith in the Appendix.

The present Appeal Brief is in furtherance of the Notice of Appeal filed in this case on May 3, 2005.

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The Commissioner is authorized to charge payment of any additional fee required in connection with this appeal to Deposit Account No. 12-2252.

This Appeal Brief is filed in triplicate as required under 37 CFR §1.192(a).

This brief contains the following items under the following headings and in the order set forth below (37 CFR 1.192(c)):

- I. Real Party in Interest;
- II. Related Appeals and Interferences;
- III. Status of Claims;
- IV. Status of the Amendments;
- V. Summary of the Invention;
- VI. Issues;
- VII. Grouping of Claims;
- VIII. Argument;
- IX. Appendix of Claims Involved in the Appeal; and
- X. Conclusion.

The final page of this brief bears the attorney's signature.

I. REAL PARTY IN INTEREST (37 CFR 1.192(c)(1))

The real party in interest is the Assignee of the present patent application, LSI Logic Corporation, a corporation organized and existing under the laws of the State of Delaware, having its principal place of business at 1621 Barber Lane, Milpitas, California 95035.

II. RELATED APPEALS AND INTERFERENCES (37 CFR 1.192(c)(2))

There are no other pending, related appeals or interferences known to the Appellant, Appellant's legal representative, or Assignee which will directly affect, be directly affected by, or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF THE CLAIMS (37 CFR 1.192(c)(3))

There are seven (7) claims in the present application, claims 1-7. Claims 1-7 stand finally rejected and are on appeal.

IV. STATUS OF THE AMENDMENTS (37 CFR 1.192(c)(4))

A Response to the Office Action dated February 8, 2005 was filed on March 16, 2005. The Amendment was considered by the Examiner and an Advisory Action Before the Filing of an Appeal Brief was issued by the Examiner on April 5, 2005. A Supplemental Response to the Office Action dated February 8, 2005 was filed on April 29, 2005. The Notice of Appeal was timely filed on May 3, 2005.

V. SUMMARY OF THE INVENTION (37 CFR 1.192(c)(5))

As discussed at page 10, lines 18-19 and page 11, lines 1-8 of the specification, the present invention relates to a method of forming an interconnect in a substrate 10 which includes one or more dielectric layers 12, 14, 16 and a copper deposit 18, said method comprising: forming a trench 20 in the substrate; forming a via 22 in the substrate to the copper deposit 18; depositing an interconnect liner layer of aluminum-0.5% copper alloy 24 in the trench 20 and via

22; depositing copper 26 onto the aluminum-0.5% copper alloy 24 interconnect liner layer; and polishing the copper 26, wherein the interconnect liner layer is a permanent component of the interconnect and does not interact with the copper 26 or copper deposit to form an alloy at any time while the method is performed.

As discussed at page 11, lines 16-19 and page 12, lines 1-7 of the specification, the present invention also relates to an interconnect in a substrate 10 which includes one or more dielectric layers 12, 14, 16, said interconnect comprising a first copper deposit, a second copper deposit, and an aluminum-0.5% copper alloy interconnect liner 24 disposed between and in contact with the first and second copper deposits and between the second copper deposit and at least one of the dielectric layers 12, 14, 16, wherein the interconnect liner is a permanent component of the interconnect and is not combined with either of the copper deposits to form an alloy.

VI. ISSUES (37 CFR 1.192(c)(6))

1. Whether claims 1-7 are patentable over the Examiner's rejection under 35 U.S.C. §102(b) as being unpatentable over United States Patent No. 6,204,179 to McTeer.

2. Whether claims 1-7 are patentable over the Examiner's rejection under 35 U.S.C. §103(a) as being unpatentable over United States Patent No. 6,204,179 to McTeer and in view of United States Patent No. 6,150,252 to Hsu et al.

VII. GROUPING OF CLAIMS (37 CFR 1.192(c)(7))

All of the claims being appealed stand or fall together.

VIII. ARGUMENT (37 CFR 1.192(c)(8))

The issue under 35 U.S.C. § 102(b) is whether claims 1-7 are patentable over United States Patent No. 6,204,179 to McTeer. The issue under 35 U.S.C. § 103(a) is whether claims 1-7 are patentable over United States Patent No. 6,204,179 to McTeer in view of United States Patent No. 6,150,252 to Hsu et al. as asserted by the Examiner.

The independent claims specifically claim a permanent interconnect liner layer of aluminum-0.5% copper alloy. The major target of the present invention is to create an additional metal liner between the diffusion barrier (Ta/TaN) and the copper inside the vias and trenches. This liner should be characterized by a good electrical conductivity and at the same time by a good enough resistivity to the electromigration. This liner should survive during the chip lifetime. The present application claims using aluminum-0.5% copper alloy as the material for this liner.

In contrast, United States Patent No. 6,204,179 (McTeer) uses a sacrificial Al liner as a wetting underlayer to assist a gap-fill by copper reflow. McTeer needs this Al to lower the Cu reflow temperature (to prevent diffusion barrier material from the chemical erosion). As mentioned in column 18, lines 15-18, "...the aluminum wetting layer is consumed thereby forming a Cu_{sub}_nAl alloy layer wherein n is an integer from about 0.5 to about 4". The Examiner has determined that this means 0.5% copper alloy, however, one having ordinary skill in the art would interpret McTeer, and specifically column 18, lines 15-18 of McTeer, to mean that the alloy is from interval of atomic compositions: from 2Al - 1Cu to 1Al - 4Cu, which means an alloy with Cu concentration from 33% to 80%, but not 0.5%. This assertion has been presented to the Examiner, along with a supporting Declaration from one of the inventors, a copy

of which is enclosed herewith to support this appeal.

To one having ordinary skill in the art, it is clear why McTeer needs such alloys. The melting point will be reduced almost twice when 40-50% of Al will be added to Cu (compared with the Cu melting point). In the present invention, this Cu concentration is not acceptable because it will dramatically increase a resistivity of the Al liner and will destroy the purpose of its employment.

United States Patent No. 6,150,252 (Hsu et al.) does not disclose or suggest a copper fill. In addition to specifically claiming a permanent interconnect liner layer of aluminum-0.5% copper alloy, the independent claims of the present invention specifically claim a copper fill. In contrast, Hsu et al. discloses filling with aluminum (see col. 9, lines 1-10).

An additional very important point that should be taken into account when comparing the present invention to McTeer and Hsu et al. is the complete difference in copper technology that is employed in the present invention.

A prior-art reference is analogous if

- (1) the art is from the same field of endeavor, regardless of the problem addressed; and
- (2) if not from the same field of endeavor, whether it is still reasonably pertinent to the particular problem to be solved.

E.g., In re Clay, 966 F.2d 656, 658-59, 23 U.S.P.Q2d 1058, 1060 (Fed. Cir. 1992); MPEP Section 2141.01(a). But just because the two references at issue in this case relate to interconnects, does not mean they are from the same field of endeavor. For example, in the *Clay* case, the Office argued that the prior art patent and the application at issue were part of a

common endeavor: maximizing withdrawal of petroleum stored in petroleum reservoirs. The Court held that the art is not within the same field of endeavor merely because both relate to the petroleum industry. The application at issue was for storage of refined liquid hydrocarbons; the prior art patent was for the extraction of crude petroleum. *In re Clay, supra*, at 659, 23 U.S.P.Q.2d at 1060.

Similarly, in *Wang Laboratories Inc. v. Toshiba Corp.*, 993 F.2d 858, 26 U.S.P.Q.2d 1767 (Fed. Cir. 1993), cited at Section 2141.01(a) of the MPEP, the patents-in-suit were for single in-line memory modules. The prior art at issue was for single in-line memory modules. The Federal Court stated, nonetheless:

The Allen-Bradley art *is not in the same field of endeavor as the claimed subject matter merely because it relates to memories*. It involves memory circuits in which modules of varying sizes may be added or replaced; in contrast, the subject patents teach compact modular memories.

Id. at 864, 26 U.S.P.Q.2d at 1773 (emphasis added). Even though both the application and the prior art reference described SIMMs, they were still different fields of endeavor.

McTeer and Hsu et al. are similarly not in the same field of endeavor as the present invention. The present invention uses a standard dual damascene copper process, where copper is deposited by the electroplating (current standard). Everything that the present invention proposes is the introduction of an additional process step, which is a PVD-based deposition of Al-0.5% Cu liner on the top of the deposited diffusion barrier (TaN), in the standard process flow. McTeer has used the PVD technique for copper deposition, and this is a reason why McTeer needs to introduce a copper reflow step and to deposit a sacrificial Al liner.

Hsu et al. uses a high pressure processing for cavity filling. It is a two-step process:

deposition of a thin liner, followed by deposition of a thicker layer to close the mouth of the cavity and high pressure processing to force the fill layer further into the cavity to complete cavity filling. (column 2, lines 55-58). Hsu et al. needs the first liner for wetting purposes only.

Applicant respectfully submits that neither McTeer nor Hsu et al. disclose or suggest providing an aluminum-0.5% copper alloy interconnect liner layer in contact with a copper fill.

In view of the above amendments and remarks, Applicant respectfully submits that the claims are allowable over the prior art of record, and respectfully requests that the application be passed to issuance.

As discussed above, a Declaration from one of the inventors is enclosed herewith. Said Declaration is hereby incorporated herein by reference in its entirety, to support the position taken in this Appeal Brief.

IX. APPENDIX OF CLAIMS INVOLVED IN THE APPEAL (37 CFR 1.192(c)(9))

1. A method of forming an interconnect in a substrate which includes one or more dielectric layers and a copper deposit, said method comprising: forming a trench in the substrate; forming a via in the substrate to the copper deposit; depositing an interconnect liner layer of aluminum-0.5% copper alloy in the trench and via; depositing copper onto the aluminum-0.5% copper alloy interconnect liner layer; and polishing the copper, wherein the interconnect liner layer is a permanent component of the interconnect and does not interact with the copper or copper deposit to form an alloy at any time while the method is performed.

2. A method as recited in claim 1, wherein the step of depositing a layer of aluminum-0.5% copper alloy comprises using a PVD technique.

3. A method of forming an interconnect in a substrate which includes one or more dielectric layers and a copper deposit, said method comprising: forming a trench in the substrate; forming a via in the substrate to the copper deposit; depositing an intermediate liner layer in the trench and via and on the copper deposit; depositing an interconnect liner layer of aluminum-0.5% copper alloy on the intermediate layer; depositing copper onto the aluminum-0.5% copper alloy; and polishing the copper, wherein the interconnect liner layer is a permanent component of the interconnect and does not interact with the copper or copper deposit to form an alloy at any time while the method is performed.

4. A method as recited in claim 3, wherein the step of depositing a layer of aluminum-0.5% copper alloy comprises using a PVD technique.

5. A method as recited in claim 3, wherein the step of depositing an intermediate liner layer comprises depositing Ta/TaN.

6. An interconnect in a substrate which includes one or more dielectric layers, said interconnect comprising a first copper deposit, a second copper deposit, and an aluminum-0.5% copper alloy interconnect liner disposed between and in contact with the first and second copper deposits and between the second copper deposit and at least one of the dielectric layers, wherein the interconnect liner is a permanent component of the interconnect and is not combined with either of the copper deposits to form an alloy.

7. An interconnect as recited in claim 6, wherein the aluminum-copper alloy interconnect liner has been deposited using a PVD technique.

X. CONCLUSION

In summary, the prior art cited by the Examiner does not anticipate or render obvious the claims of the present invention because it does not disclose or suggest providing an aluminum-0.5% copper alloy interconnect liner layer in contact with a copper fill.

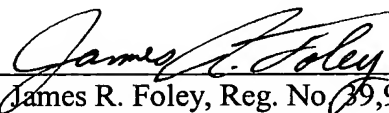
Therefore, Appellant respectfully requests that the Board:

1. Direct the Examiner to withdraw the rejection of claims 1-7 in the application under 35 U.S.C. § 102(b) and 35 U.S.C. § 103(a).
2. Direct the Examiner to proceed with issuance of the present application.

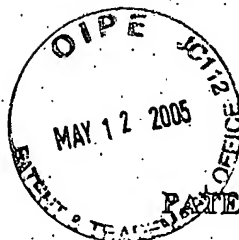
This Appeal Brief is respectfully submitted by:

Attorneys for Applicant/Appellant

Date: May 10, 2005

By: 
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PATENT

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DAMASCENE INTERCONNECT)
WITH IMPROVED RELIABILITY)
Inventors: Valeriy Sukharev et al.)
Examiner: Jesse A. Fenty)
Art Unit: 2815)
Atty. Ref.: 03-0509)

DECLARATION OF VALERIY SUKHAREV
IN SUPPORT OF OFFICE ACTION RESPONSE

1. I am one of the inventors of the above-identified patent application.
2. I have a Ph.D. degree from KARPOV INSTITUTE OF PHYSICAL CHEMISTRY, MOSCOW, RUSSIA, and I have 10 years experience in the semiconductor industry.
3. The independent claims of the above-identified application have been amended to specifically claim a permanent interconnect liner layer of aluminum-0.5% copper alloy. The major target of the present invention is to create an additional metal liner between the diffusion barrier (Ta/TaN) and the copper inside the vias and trenches. This liner should be characterized by a good electrical conductivity and at the same time by a good enough resistivity to the electromigration. This liner should survive during the chip lifetime. The present application claims using aluminum-0.5% copper alloy as the material for this liner.
4. In contrast, United States Patent No. 6,204,179 (McTeer) uses a sacrificial Al liner as a wetting underlayer to assist a gap-fill by copper reflow. McTeer needs this Al to lower the Cu reflow temperature (to prevent diffusion barrier material from the chemical erosion). As mentioned in column 18, lines 15-18, "...the aluminum wetting layer is consumed thereby forming a Cu_nAl alloy layer wherein n is an integer from about 0.5 to about 4". The Examiner has determined that this means 0.5% copper alloy, however, one having ordinary skill in the art would interpret McTeer, and specifically column 18, lines 15-18 of McTeer, to mean that the alloy is from interval of atomic compositions: from 2Al - 1Cu to 1Al - 4Cu, which means an alloy with Cu concentration from 33% to 80%, but not 0.5%.

5. To one having ordinary skill in the art, it is clear why McTeer needs such alloys. The melting point will be reduced almost twice when 40-50% of Al will be added to Cu (compared with the Cu melting point). In the present invention, this Cu concentration is not acceptable because it will dramatically increase a resistivity of the Al liner and will destroy the purpose of its employment.
6. United States Patent No. 6,150,252 (Hsu et al.) does not disclose or suggest a copper fill. In addition to specifically claiming a permanent interconnect liner layer of aluminum-0.5% copper alloy, the independent claims of the present invention specifically claim a copper fill. In contrast, Hsu et al. discloses filling with aluminum (see col. 9, lines 1-10).
7. An additional very important point that should be taken into account when comparing the present invention to McTeer and Hsu et al. is the complete difference in copper technology that is employed in the present invention. The present invention uses a standard dual damascene copper process, where copper is deposited by the electroplating (current standard). Everything that the present invention proposes is the introduction of an additional process step, which is a PVD-based deposition of Al-0.5% Cu liner on the top of the deposited diffusion barrier (TaN), in the standard process flow. McTeer has used the PVD technique for copper deposition, and this is a reason why McTeer needs to introduce a copper reflow step and to deposit a sacrificial Al liner.
8. Hsu et al. uses a high pressure processing for cavity filling. It is a two-step process: deposition of a thin liner, followed by deposition of a thicker layer to close the mouth of the cavity and high pressure processing to force the fill layer further into the cavity to complete cavity filling. (column 2, lines 55-58). Hsu et al. needs the first liner for wetting purposes only.

As a person signing below:

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

SIGNATURE

Inventor's Full Name (Printed) Valeriy Sukharev

Inventor's Signature V. Sukhar

Date 04/28/05